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APPLICATION FOR LETTERS PATENT

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**Methods Of Forming A Base Plate For A Field
Emission Display (FED) Device, Methods Of
Forming A Field Emission Display (FED) Device,
Base Plates For Field Emission Display (FED)
Devices, And Field Emission Display (FED) Devices**

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INVENTOR

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1 **METHODS OF FORMING A BASE PLATE FOR A FIELD**
2 **EMISSION DISPLAY (FED) DEVICE, METHODS OF FORMING A**
3 **FIELD EMISSION DISPLAY (FED) DEVICE, BASE PLATES FOR**
4 **FIELD EMISSION DISPLAY (FED) DEVICES, AND FIELD**
5 **EMISSION DISPLAY (FED) DEVICES**

6 **PATENT RIGHTS STATEMENT**

7 This invention was made with Government support under Contract
8 No. DABT63-97-C-0001 awarded by Advanced Research Projects Agency
9 (ARPA). The Government has certain rights in this invention.

10 **TECHNICAL FIELD**

11 This invention relates to methods of forming a base plate for a
12 field emission display (FED) device, to methods of forming a field
13 emission display (FED) device, to base plates for field emission
14 display (FED) devices, and to field emission display (FED) devices.

15 **BACKGROUND OF THE INVENTION**

16 Flat-panel displays are widely used to visually display information
17 where the physical thickness and bulk of a conventional cathode ray
18 tube is unacceptable or impractical. Portable electronic devices and
19 systems have benefitted from the use of flat-panel displays, which
20 require less space and result in a lighter, more compact display system
21 than provided by conventional cathode ray tube technology.

22 The invention described below is concerned primarily with field
23 emission flat-panel displays or FEDs. In a field emission flat-panel
24 display, an electron emitting cathode plate is separated from a display

1 face or face plate at a relatively small, uniform distance. The
2 intervening space between these elements is evacuated. Field emission
3 displays have the outward appearance of a CRT except that they are
4 very thin. While being simple, they are also capable of very high
5 resolutions. In some cases they can be assembled by use of technology
6 already used in integrated circuit production.

7
8 Field emission flat-panel displays utilize field emission devices, in
9 groups or individually, to emit electrons that energize a
10 cathodoluminescent material deposited on a surface of a viewing screen
11 or display face plate. The emitted electrons originate from an emitter
12 or cathode electrode at a region of geometric discontinuity having a
13 sharp edge or tip. Electron emission is induced by application of
14 potentials of appropriate polarization and magnitude to the various
15 electrodes of the field emission device display, which are typically
16 arranged in a two-dimensional matrix array.

17
18 Field emission display devices differ operationally from cathode ray
19 tube displays in that information is not impressed onto the viewing
20 screen by means of a scanned electron beam, but rather by selectively
21 controlling the electron emission from individual emitters or select
22 groups of emitters in an array. This is commonly known as "pixel
23 addressing." Various displays are described in U.S. Patent
24 Nos. 5,655,940, 5,661,531, 5,754,149, 5,563,470, and 5,598,057 the
disclosures of which are incorporated by reference herein.

Fig. 1 illustrates a cross-sectional view of an exemplary field emission display (FED) device 10. Device 10 comprises a face plate 12, a base plate 14, and spacers 16 extending between base plate 14 and face plate 12 to maintain face plate 12 in spaced relation relative to base plate 14. Face plate 12, base plate 14 and spacers 16 can comprise, for example, glass. Phosphor regions 18, 20, and 22 are associated with face plate 12, and separated from face plate 12 by a transparent conductive layer 24. Transparent conductive layer 24 can comprise, for example, indium tin oxide or tin oxide. Phosphor regions 18, 20, and 22 comprise phosphor-containing masses. Each of phosphor regions 18, 20, and 22 can comprise a different color phosphor. Typically, the phosphor regions comprise either red, green or blue phosphor. A black matrix material 26 is provided to separate phosphor regions 18, 20, and 22 from one another.

Base plate 14 has emitter regions 28, 30 and 32 associated therewith. The emitter regions comprise emitters or field emitter tips 34 which are located within radially symmetrical apertures 36 (only some of which are labeled) formed through a conductive gate layer 38 and a lower insulating layer 40. Emitters 34 are typically about 1 micron high, and are separated from base plate 14 by a conductive layer 42. Emitters 34 and apertures 36 are connected with circuitry (not shown) enabling column and row addressing of the emitters 34 and apertures 36, respectively.

1 A voltage source 44 is provided to apply a voltage differential
2 between emitters 34 and surrounding gate apertures 36. Application of
3 such voltage differential causes electron streams 46, 48, and 50 to be
4 emitted toward phosphor regions 18, 20, and 22 respectively.
5 Conductive layer 24 is charged to a potential higher than that applied
6 to gate layer 38, and thus functions as an anode toward which the
7 emitted electrons accelerate. Once the emitted electrons contact
8 phosphor dots associated with regions 18, 20, and 22 light is emitted.
9 As discussed above, the emitters 34 are typically matrix addressable via
10 circuitry. Emitters 34 can thus be selectively activated to display a
11 desired image on the phosphor-coated screen of face plate 12.

12 The face plate typically has red, green and blue phosphor regions
13 with black matrix areas 26 surrounding the phosphor regions. The
14 three phosphor colors (red, green, and blue) can be utilized to generate
15 a wide array of screen colors by simultaneously stimulating one or more
16 of the red, green and blue regions.

17 As displays such as the one described above continue to grow in
18 size and complexity, challenges are posed with respect to their design.
19 For example, small-sized FED devices typically have a high resolution.
20 As such displays grow in size, such resolution is desired to be
21 maintained or even improved, yet challenges exist because of the
22 increased dimensions. One such challenge is manifest in the video rate
23 requirement in larger-area displays. The video rate requirement is
24 typically determined by the RC time constant of the device. Typically,

1 address lines (e.g., row and column address lines) extend the entire
2 length or width dimension respectively, of the addressable matrix of field
3 emitters. Larger displays call for larger matrices. With larger matrices,
4 such address lines can extend for greater lengths. Such greater lengths,
5 accordingly, carry with them higher RC time constants which adversely
6 impact the video rate requirement. Other challenges in the design of
- the larger-area display will be apparent to those of skill in the art.

8 One solution which has been proposed in the past (see, e.g. U.S.
9 Patent No. 5,655,940) is to provide separate emitter plates which are
10 subsequently mounted on a substrate to provide a larger-area display.
11 This approach, however, can be inadequate and can result in much
12 more processing complexity than is desirable. Specifically, multiple
13 emitter plates must be separately formed and positioned relative to one
14 another on a substrate. The plates must be precisely positioned to
15 avoid anomalies in the subsequently rendered image. Needless to say,
16 this can be a time-consuming process and results in more processing
17 complexity than is desirable.

18 Accordingly, this invention arose out of concerns associated with
19 providing improved field emission display (FED) devices and methods
20 of forming such devices. This invention also arose out of concerns
21 associated with providing larger-area FED displays with little or no
22 additional processing complexity.
23
24

SUMMARY OF THE INVENTION

Methods of forming base plates for field emission display (FED) devices, methods of forming field emission display (FED) devices, and resultant FED base plate and device constructions are described. In one embodiment, a substrate is provided and is configurable into a base plate for a field emission display. A plurality of discrete, segmented regions of field emitter tips are formed by at least removing portions of the substrate. The regions are electrically isolated into separately-addressable regions. In another embodiment, a plurality of field emitters are formed from material of the substrate and arranged into more than one demarcated, independently-addressable region of emitters. Address circuitry is provided and is operably coupled with the field emitters and configured to independently address individual regions of the emitters. In yet another embodiment, a monolithic addressable matrix of rows and columns of field emitters is provided and has a perimetral edge defining length and width dimensions of the matrix. The matrix is partitioned into a plurality of discretely-addressable sub-matrices of field emitters. Row and column address lines are provided and are operably coupled with the matrix and collectively configured to address the field emitters. At least one of the row or column address lines has a length within the matrix which is sufficient to address less than all of the field emitters which lie in the direction along which the address line extends within the matrix.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a side sectional view of a portion of an exemplary field emission display (FED) device which can be constructed in accordance with one or more embodiments of the present invention.

Fig. 2 is a somewhat schematic view of a FED base plate and address circuitry in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 2, and in accordance with one embodiment of the present invention, a substrate 52 is provided and is configurable into a base plate for a field emission display (FED). In the illustrated example, substrate 52 corresponds to base plate 14 of Fig. 1. A plurality of discrete, segmented regions of field emitter tips (such as field emitters or emitter tips 34 in Fig. 1) are formed by removing portions of the substrate, preferably through known etching techniques. Exemplary discrete, segmented regions are shown in Fig. 2 at 54, 56, 58 and 60. In a preferred embodiment, regions 54-60 are electrically isolated from one another into separately-addressable regions of field

1 emitter tips. In the illustrated and preferred embodiment, four regions
2 are formed. It is possible, however, for different numbers of regions
3 to be formed. For example, in one embodiment at least two regions
4 are formed. In another embodiment, at least three regions are formed.
5 More than four regions can be formed, e.g. six, eight, ten, twelve and
6 the like. Additionally, other than even numbers of regions can be
- formed as, for example, three, five, seven and the like.

8 In another embodiment, formation of the discrete, segmented
9 regions comprises etching the substrate into the formed regions. In a
10 preferred embodiment, the base plate, as formed, comprises a monolithic
11 base plate of field emitter tips. By providing a monolithic base plate
12 with the plurality of discrete, segmented regions, advantages are achieved
13 over prior devices. For example, the monolithic nature of various of
14 the preferred embodiments can reduce processing complexities by
15 requiring processing of only one work piece, e.g. substrate 52, in order
16 to form the base plate. In addition, resolution of the ultimately-formed
17 device can be improved because of the uniformity of the material from
18 which the base plate is formed. Specifically, by forming the illustrated
19 discrete, segmented, and electrically-isolated regions from a common
20 substrate, uniformity in the ultimately provided image can be enhanced.

21 In another embodiment, address circuitry is provided and operably
22 coupled with substrate 52. Preferably, the address circuitry is configured
23 to separately address individual regions of the field emitter tips. In the
24 illustrated example of Fig. 2, the address circuitry comprises row drivers

1 and column drivers. Each individual region has its own row driver and
2 column driver. Individual row and column drivers are arranged in
3 groupings designated at 62, 64, 66, and 68 for each individual region.
4 Specifically, the row and column drivers in grouping 62 are provided for
5 addressing region 54; the row and column driver in grouping 64 are
6 provided for addressing region 56; the row and column driver in
7 grouping 66 are provided for addressing region 60; and the row and
8 column driver in grouping 68 are provided for addressing region 58.
9 The individual row and column drivers are connected with individual row
10 and column lines which extend through the individual regions. The row
11 and column lines are typically formed by depositing a conductive
12 material, and then using a photomask to define the conductive line
13 patterns which are subsequently etched from the conductive material.
14 Here, in order to form the separately-addressable regions, the photomask
15 is modified such that the subsequently-etched row and column lines do
16 not extend across the entirety of the addressable matrix, but rather only
17 partially across the matrix in regions corresponding to those illustrated
18 in Fig. 2.

19 In one embodiment, a face plate, such as face plate 12 in Fig. 1,
20 is provided and supports areas of luminescent material. Exemplary
21 luminescent material areas are shown at 18, 20, and 22. Face plate 12
22 is preferably mounted in operable proximity with substrate 52 to provide
23 a field emission display (FED) device.
24

1 In another embodiment, a plurality of field emitters, such as
2 emitters 34 in Fig. 1, are formed from material of the substrate, which,
3 in this example, corresponds to substrate 14. The emitters are arranged
4 into more than one demarcated, independently-addressable region of
5 emitters. Exemplary demarcated, independently-addressable regions are
6 shown in Fig. 2 at 54, 56, 58, and 60. Demarcation of the individual
7 regions occurs along lines 70, 72. Address circuitry, such as that
8 described above, is preferably provided and operably coupled with the
9 field emitters and configured to independently address the individual
10 regions of emitters. In one embodiment, the emitters are arranged into
11 more than two demarcated, independently-addressable regions of emitters.
12 In another embodiment, the emitters are arranged into more than three
13 demarcated, independently-addressable regions of emitters. In a
14 preferred embodiment, the emitters are arranged into four demarcated,
15 independently-addressable regions of emitters. In the illustrated example,
16 demarcation of the individual regions of emitters takes place by forming
17 address lines, e.g. row and column lines which are effectively contained
18 within the individual respective regions, and which do not extend into
19 any other individual region. Such can be accomplished by using a
20 photomask which defines the individual address lines within each region.

21 In another embodiment, the arrangement of emitters defines a
22 plurality of rows and columns within each region. In this example,
23 portions of exemplary rows and columns are schematically shown within
24 each of regions 54-60 as cross-hatched areas. In this example, provision

1 of the address circuitry comprises providing at least two separate row
2 drivers for addressing rows in different regions of the emitters. For
3 example, in the illustrated example, region 54 has its own row driver
4 which comprises part of grouping 62. Similarly, region 56 has its own
5 row driver which comprises part of grouping 64. In another
6 embodiment, provision of the address circuitry comprises providing at
7 least two separate column drivers for addressing columns in different
8 regions of the emitters. For example, region 54 has its own column
9 driver which comprises part of grouping 62. Likewise, region 56 has
10 its own column driver which comprises part of grouping 64. In a
11 preferred embodiment, provision of the address circuitry comprises
12 providing at least two separate row drivers and at least two separate
13 column drivers for addressing the rows and columns in different
14 respective regions of the emitters. In the illustrated example, four
15 exemplary regions, i.e. regions 54-60, are provided. Each region has its
16 own row driver and column driver.

17 In another embodiment, a monolithic addressable matrix of rows
18 and columns of field emitters is provided. In this example, the
19 monolithic addressable matrix corresponds to substrate 52 of Fig. 2.
20 The matrix has a perimetral edge 74 which defines length and width
21 dimensions L, W respectively, of the matrix. The matrix is partitioned
22 into a plurality of discretely-addressable sub-matrices of field emitters.
23 Exemplary sub-matrices are shown at 54, 56, 58, and 60. Row and
24 column address lines are provided and are operably coupled with the

1 matrix. The row and column address lines (shown schematically as
2 cross-hatched areas in each of the regions) are collectively configured
3 to address the field emitters in each region. At least one of the row
4 or column address lines has a length within the matrix which is
5 sufficient to address less than all of the field emitters which lie in the
6 direction along which the address line extends within the matrix. As
7 an illustrative example, consider row address line R_x in sub-matrix 58.
8 Row address line R_x extends in a direction A within the matrix defined
9 by perimetral edge 74. Row address line R_x has a length within the
10 matrix defined by the perimetral edge which is sufficient to address less
11 than all of the field emitters which lie in the direction along which line
12 R_x extends within the matrix. Specifically, in this example, row address
13 line R_x can address field emitters only within sub-matrix 58, and not
14 within sub-matrix 60 which lie in a common direction with direction A.
15 The same can be said for the other row address lines and their
16 respective sub-matrices, as well as the other column address lines and
17 their sub-matrices.

18 In one embodiment, the length of the one row or column address
19 line within the matrix is less than a length (L) or width (W) dimension
20 of the matrix. In another embodiment, the length of the one row or
21 column address line within the matrix is less than a length or width
22 dimension of one of the sub-matrices.

23 In one embodiment, the partitioning of the matrix comprises
24 partitioning the matrix into more than two sub-matrices. In another

embodiment, the matrix is partitioned into more than three sub-matrices. In a preferred embodiment, the matrix is partitioned into four sub-matrices.

In yet another embodiment, a field emission display (FED) face plate comprises a monolithic substrate configured into a base plate for a field emission display (FED). The base plate comprises a plurality of regions of field emitter tips which comprise material of the substrate. Individual regions of the plurality of regions are discrete and electrically isolated from one another and are configured to be separately addressed. An exemplary base plate is shown in Fig. 2 at 52. In one embodiment, the substrate comprises at least two regions of field emitter tips. In another embodiment, the substrate comprises at least three regions of field emitter tips. In a preferred embodiment, the substrate comprises at least four regions of field emitter tips.

Various advantages can be achieved by the embodiments described above. Improvements can be achieved in the refresh rates of the ultimately-formed FED devices which are faster than those of identical displays with non-partitioned base plates. This is because the RC time constant scales linearly with the length of the address lines, i.e. row and column address lines. In addition, larger displays can be constructed for applications where a large viewing area is desired, such as an engineering work station or for presentations to larger groups of people in a conference room setting. Additionally, higher resolution can be achieved in larger displays which is comparable with the resolution in

1 smaller displays. Moreover, multiple images can be viewed and updated
2 independently of other images.

3 In compliance with the statute, the invention has been described
4 in language more or less specific as to structural and methodical
5 features. It is to be understood, however, that the invention is not
6 limited to the specific features shown and described, since the means
- herein disclosed comprise preferred forms of putting the invention into
8 effect. The invention is, therefore, claimed in any of its forms or
9 modifications within the proper scope of the appended claims
10 appropriately interpreted in accordance with the doctrine of equivalents.
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